REMARKS

Claims 2, 4-7, 9, 11-13, 15, 17, 19-22, 24, 26, 27, 29-36, and 38-43 are pending in the present application.

In the office action mailed February 25, 2005 (the "Office Action"), claims 9, 2, 5-7, 17, and 24 were rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,953,015 to Choi (the "Choi patent"). Claims 4, 11-13, 15, and 19-22 were rejected under 35 U.S.C. 103(a) as being unpatentable over the Choi patent in view of National Semiconductor, "Easy Logarithms for COP400" (the "NS reference"). Claims 26, 27, 30, 32-36, and 39-43 were rejected under 35 U.S.C. 103(a) as being unpatentable over the Choi patent in view of U.S. Patent No. 6,292,191 to Vaswani *et al.* (the "Vaswani patent"). Claims 29 and 38 were rejected under 35 U.S.C. 103(a) as being unpatentable over the Choi patent in view of the Vaswani patent and further in view of the NS reference.

The Choi patent describes a circuit and method for determining the level-of-detail ("LOD") for texture mapping in computer graphics. Computation of the LOD is made faster, by using equation (4), at col. 3, lines 46-48, repeated here:

$$LOD = \max\left\{\left(\frac{1}{2}\right)\log_2\left[(\partial u/\partial x)^2 + (\partial v/\partial x)^2\right], \left(\frac{1}{2}\right)\log_2\left[(\partial u/\partial y)^2 + (\partial v/\partial y)^2\right]\right\} \qquad (4)$$

The circuit includes a look-up table ("LUT") 210 storing precalculated values of a simplified function for a LOD calculation to provide faster and simpler computation of the LOD. *See* Figure 2 and col. 3, lines 49-54. As described in the Choi patent, the gradients between texels of a texture map and pixels of a display coordinate system are provided to multiplexers 220 and 224. Each of the multiplexers 220 and 224 select the gradients for an axis of the texture map related to a common axis of the display coordinate system. The values are provided to a pre-processor 240 which uses the selected gradients to calculate indices. The LUT 210 is accessed by using the indices to select which of the precalculated values are to be processed by a post-processor 250. *See* col. 3, lines 55-63. The post-processor 250 calculates partial LOD ("LODP") values which are stored in registers 260 and 262.

After the LODP values are calculated and stored, a max circuit 270 then determines the maximum of the two LODP values and provides the greater of the two LODP values as the LOD. *See* col. 4, lines 2-14. In precalculating the values of the simplified function

for storage in the LUT 210, only the values for a limited range of gradients is provided. In the event that the gradient is beyond the limited range of values stored in the LUT 210, the gradient value is scaled accordingly to select values stored in the LUT 210. *See* col. 4, lines 15-38. The post-processor 250 adjusts the LODP values in the event scaling is necessary before they are stored in the registers 260 and 262. *See* col. 4, lines 39-44.

Claims 9 and 24 are patentable over the Choi patent because the Choi patent does not teach or suggest the combination of limitations as recited by the claims. For example, the Choi patent fails to teach or suggest calculating the squares of the first and second ratios, and then selecting the greater of the squares. In the Choi patent, the logarithm is calculated prior to selecting the greater value of two values. As previously discussed, the Choi patent describes a method of calculating LOD where a pre-calculated value from the LUT 210 is provided to the post-processor 250 as the LODT value based on indices calculated by the pre-processor 240. The LODT values are calculated by taking a base-two logarithm. More specifically, as described in the Choi patent, the LODT values are calculated from equation (5), at col. 3, line 53, which is repeated here:

$$LODT(X,Y)=\left(\frac{1}{2}\right)\log_2\left(X^2+Y^2\right) \tag{5}$$

The LODT values are then processed by the post-processor 250 to generate two LODP values, one using u_x, v_x and the other using u_y, v_y. *See* col. 4, lines 6-14. That is, the two LODP values are then generated by adding the value *k*, calculated by the pre-processor 240 based on u_x, v_x and u_y, v_y, to the selected LODT values. The greater of the two LODP values calculated and stored in the registers 260 and 262 is then selected by the max circuit 270 to be provided as the LOD. The circuit described in the Choi patent carries out the LOD calculation shown in equation (4), previously described.

In contrast, claim 9 recites calculating the squares of the first and second ratios, selecting the greater of the two squares, and approximating a base-two logarithm using the selected square. Unlike the method described in the Choi patent, the selection of a value is made prior to approximating the logarithm in claim 9.

In the method described in the Choi patent, the selection of two LODP values by the max circuit 270 results from using the LUT 210 for storing precalculated values that are then

indexed to provide the LODT values. Modifying the teachings of the Choi patent to select the greater of squares of two ratios would fundamentally change the operation of the system described in the Choi patent. As previously discussed, the values that are pre-calculated and stored in the LUT 210 are the logarithm of the squares of ratios for a preset range of indices. The index used to select which of the values stored in the LUT 210, as well as the k value used for finally calculating LODP values, are based on the unsquared ratios of u_x, v_x and u_y, v_y. Squaring the ratios, selecting the larger of the squares, and then applying the larger ratio as the only value to the pre-processor 240 for calculating an index to the LUT 210 and the k value could lead to erroneous LOD values since the LOD value of the Choi circuit relies on pre-calculated values that represent only part of the ultimate calculation for LOD. It may be the case that using only the larger of the square of the ratios to calculate LOD does not correspond to the LODP value that would have been selected by the max circuit 270 if both LODP values were calculated. Consequently, modifying the Choi circuit to calculate squares of the ratios, select the larger of the squares and then approximate the logarithm for the selected square would render the circuit unfit for its intended purpose.

With respect to claim 24, claim 24 recites an apparatus to calculate LOD that is configured to calculate the squares of first and second ratios, select the greater of the squares, and then approximate a base-two logarithm of the selected square. As previously discussed with respect to claim 9, the Choi patent fails to teach or suggest the limitations.

For the foregoing reasons, claims 9 and 24 are patentable over the Choi patent, and the rejection of claims 9 and 24 under 35 U.S.C. 103(a) should be withdrawn. Claims 2 and 5-7, which depend from claim 9, and claim 17, which depends from claim 24, are similarly patentable over the Choi patent based on their dependency from a respective allowable base claim. That is, each of the dependent claims further narrows the scope of the claim from which it depends, and consequently, if a claim is dependent from an allowable base claim, the dependent claim is also allowable. Therefore, the rejection of claim, 2, 5-7, 9, 17, and 24 under 35 U.S.C. 103(a) should be withdrawn.

With respect to the rejection of claims 4, 11-13, 15, and 19-22 under 35 U.S.C. 103(a), claim 15 is patentable over the Choi patent in view of the NS reference because the

combined teachings of the Choi and NS references fail to teach or suggest the combination of limitations recited by claim 15.

For example, the Choi patent fails to teach or suggest an apparatus configured to calculate the square of the first and second ratios, select the greater of the squared ratios, and approximate a logarithm of the selected squared ratio. As previously discussed with respect to claims 9 and 24, the circuit and method described in the Choi patent precalculates values that result from logarithmic calculations of the squared ratios, which are then indexed and used to calculate two partial LOD values. One of the LODP values is selected by the max circuit 270 to be provided as the LOD value. Claim 15, in contrast, selects the greater of the square of first and second ratios, and uses the selected square of the ratio for calculating the LOD. Selection is not between two partial LODs, as in the Choi patent, but between the two squared ratios.

The NS reference has been cited by the Examiner as teaching "shifting the square of a number left by the number of leading zeros and the MSB, effectively ignoring the MSB; calculating a characteristic (integer) based on the number of characteristic bits minus the number of shifts required, effectively the [(number of integer bits - 1) - LZs]; concatenating the integer value to first number; and defining the resulting number as the integer portion." *See* the Office Action at page 5, paragraph 3a (citations omitted). Even if it is assumed that the Examiner's characterization of the NS reference is accurate, it does not make up for the deficiencies of the Choi patent, as previously discussed with respect to claims 9, 15, and 24. The teachings of the NS reference as characterized by the Examiner do not change the manner in which the Choi patent calculates LOD, which as previously discussed, does not select the greater of the squares of a first and second ratio.

For the foregoing reasons, claim 15 is patentable over the Choi patent in view of the NS reference. Claims 11-13, which depend from claim 15, are similarly patentable based on their dependency from allowable claim 15. Claim 4 is patentable based on its dependency from allowable claim 9. Claims 19-22 are patentable based on their dependency from allowable claims 24. Therefore, the rejection of claims 4, 11-13, 15, and 19-22 under 35 U.S.C. 103(a) should be withdrawn.

With respect to the rejection of claims 26, 27, 30, 32-36, and 39-43 under 35 U.S.C. 103(a), claims 26 and 35 are patentable over the Choi patent in view of the Vaswani

patent because the cited references, alone or in combination, fail to disclose or suggest the combination of limitations recited by claims 26 and 35.

Claim 26 recites a graphics processing system including a LOD computation circuit similar to the apparatus of claim 24. Claim 35 recites a computer system having a LOD computation circuit similar to the apparatus of claim 24. As previously discussed with respect to claims 9, 15, and 24, the Choi patent does not disclose selecting the greater of the squares of first and second ratios for calculating the LOD. The circuit in the Choi patent uses precalculated values stored in a LUT 210 for calculating two partial LOD values, one of which is then selected by a max circuit 270 to be provided as the final LOD. In contrast, as previously discussed with respect to claim 24, the apparatus is configured to calculate the squares of the first and second ratios, select the greater of the two squares, and then approximate a logarithm for the selected squared ratio.

The Vaswani patent has been cited by the Examiner for teaching "a bus interface for coupling to a system bus; a graphics processor coupled to the bus interface to process graphics data; address and data busses coupled to the graphics processor to transfer address and graphics data to and from the graphics processor; display logic coupled to data bus to drive a display." *See* the Office Action at page 10 (citations omitted). Even if it is assumed that the Examiner's characterization of the Vaswani patent is accurate, its teachings fail to make up for the deficiencies of the Choi patent previously discussed with respect to claims 9, 15, and 24.

For the foregoing reasons, claims 26 and 35 are patentable over the Choi patent in view of the Vaswani patent. Claims 27, 30, 32-34, which depend from claim 26, and claims 36 and 39-43, which depend from claim 35, are also patentable based on their dependency from a respective allowable base claim. Therefore, the rejection of claims 26, 27, 30, 32-36, and 39-43 under 35 U.S.C. 103(a) should be withdrawn.

Claims 29 and 38 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Choi patent in view of the Vaswani patent, and further in view of the NS reference. Claim 29 depends from allowable claim 26, and claim 38 depends from allowable claim 35. Consequently, claims 29 and 38 are patentable based on their dependency from a respective allowable base claim, and therefore, the rejection of claims 29 and 38 under 35 U.S.C. 103(a) should be withdrawn.

Claims 9, 15, 24, 26, and 35, have been amended to remove the limitations added to the claims in the previously filed response.

All of the claims pending in the present application are in condition for allowance. Favorable consideration and a timely Notice of Allowance are earnestly solicited.

Respectfully submitted,

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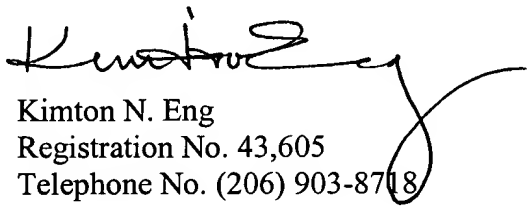

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